Problem Report PR-010

HW part: HW0001

HW rev: R002

SW rev: 2021-05-15

Test log: 20210602-FPGA RAM readout over SPI.xlsx, 20210604-FPGA RAM readout over SPI.xlsx

Description: LD not functional

Steps to reproduce the problem

1. Start test software
2. Observe the response in the SPI buffer. Reads should produce data that is different from the shift register.

Investigation notes

2021-06-02: The logic for the LD signal was incorrect. I corrected this to use the async reset input to the flip flops in spislave.v, and verified that it works.

2021-06-04: Repeated the test, without the FPGA reset pin. While it is best to drive the state machine into a known state, it should not be necessary, since the startup state of all flip flops is known at power up.